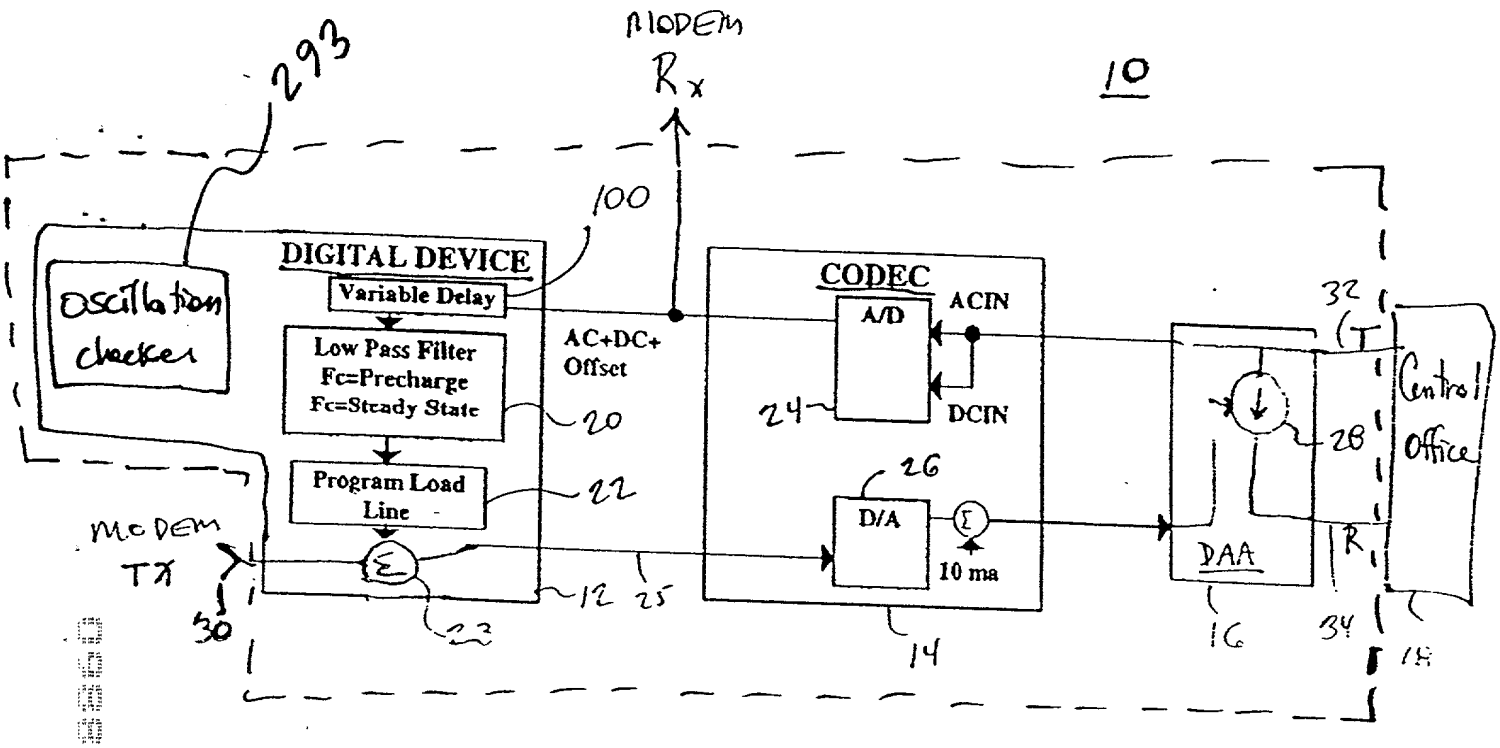


FIG. 1A

DYNAMICALLY ADJUSTABLE DIGITAL GYRATOR HAVING EXTENDED FEEDBACK

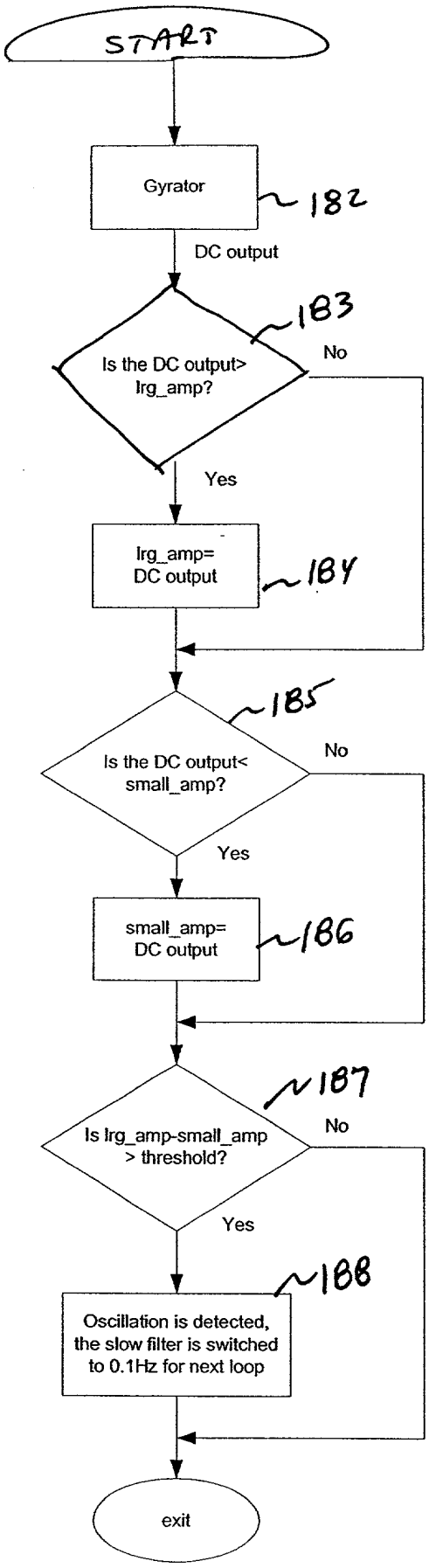

START
Gyrator
182
DC output
183
Is the DC output> Irg_amp?
No
Yes
Irg_amp= DC output
184
185
Is the DC output< small_amp?
No
Yes
small_amp= DC output
186
187
Is Irg_amp-small_amp > threshold?
No
Yes
188
Oscillation is detected, the slow filter is switched to 0.1Hz for next loop
exit

FIG. 1B

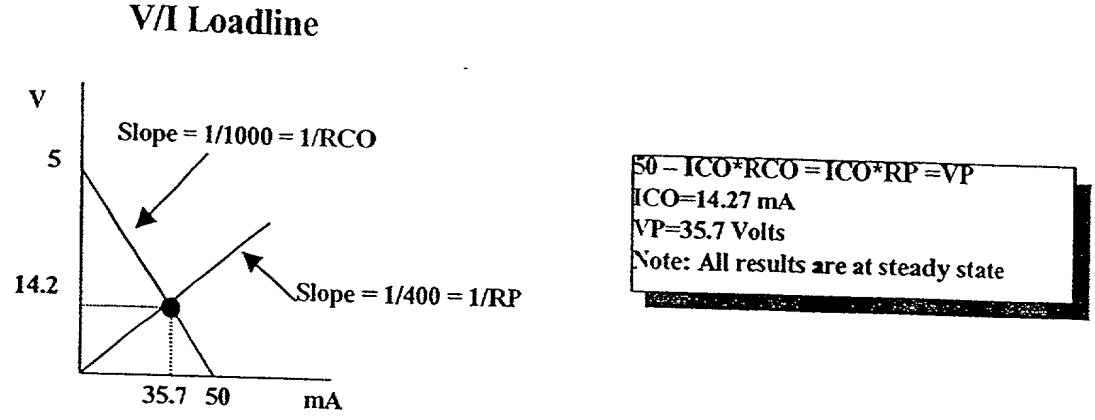
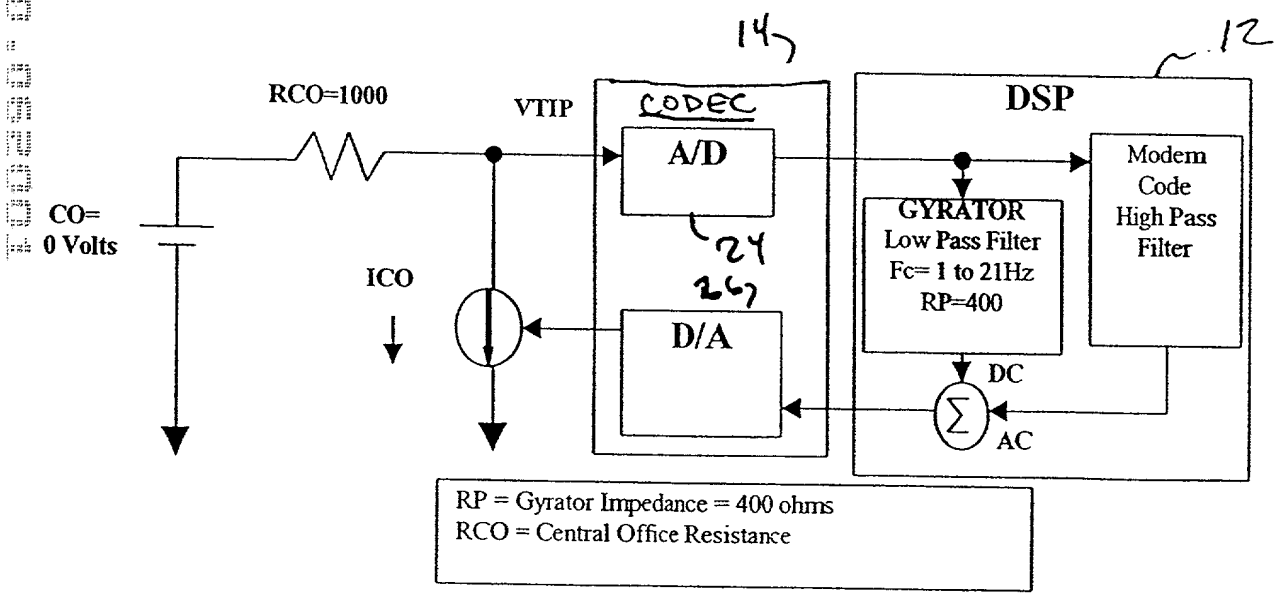


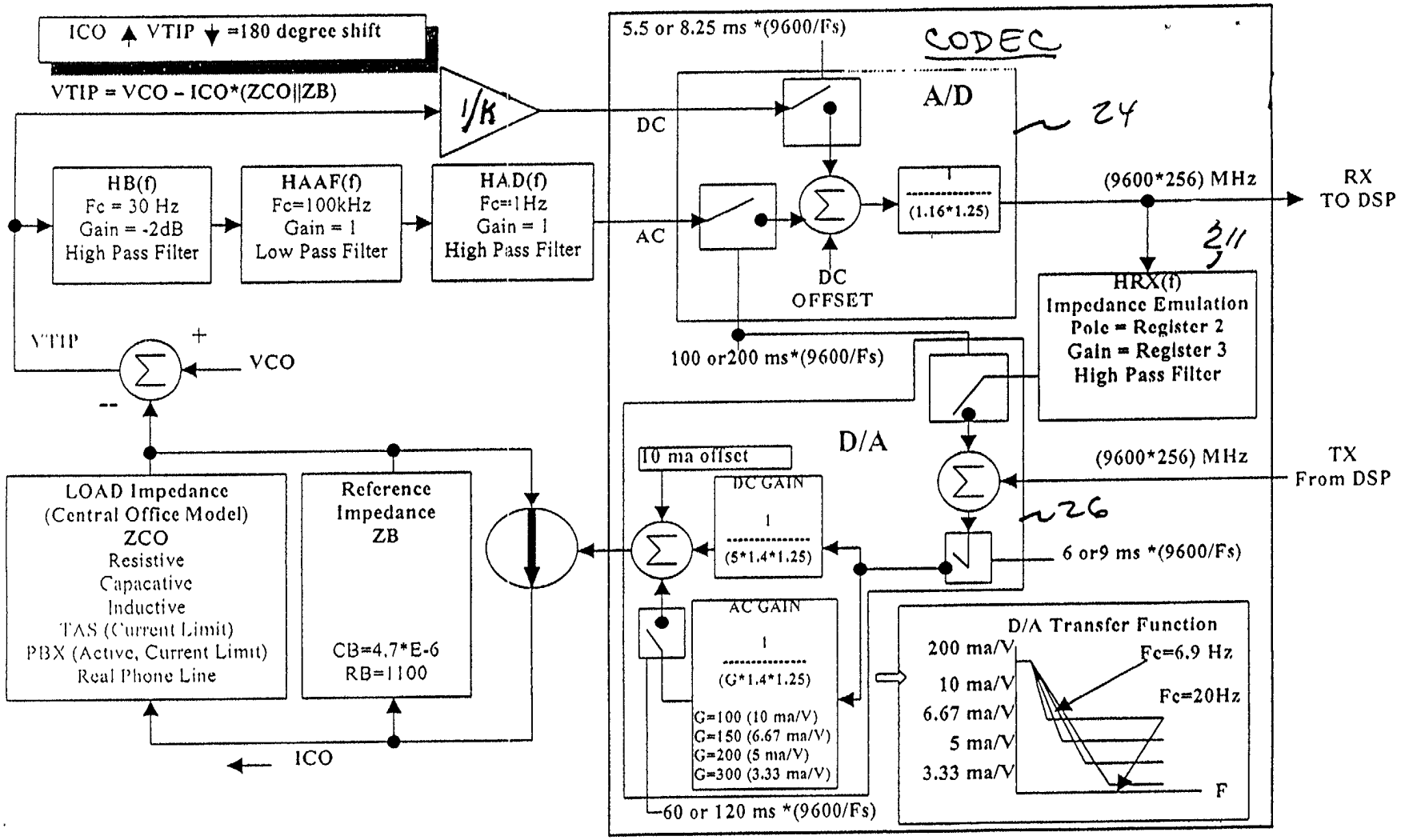
FIG. 2A



DYNAMICALLY ADJUSTABLE

Digital Gyrator Example

FIG. 2B



Codec and Telephone System Stability Block Diagram

Fig. 3

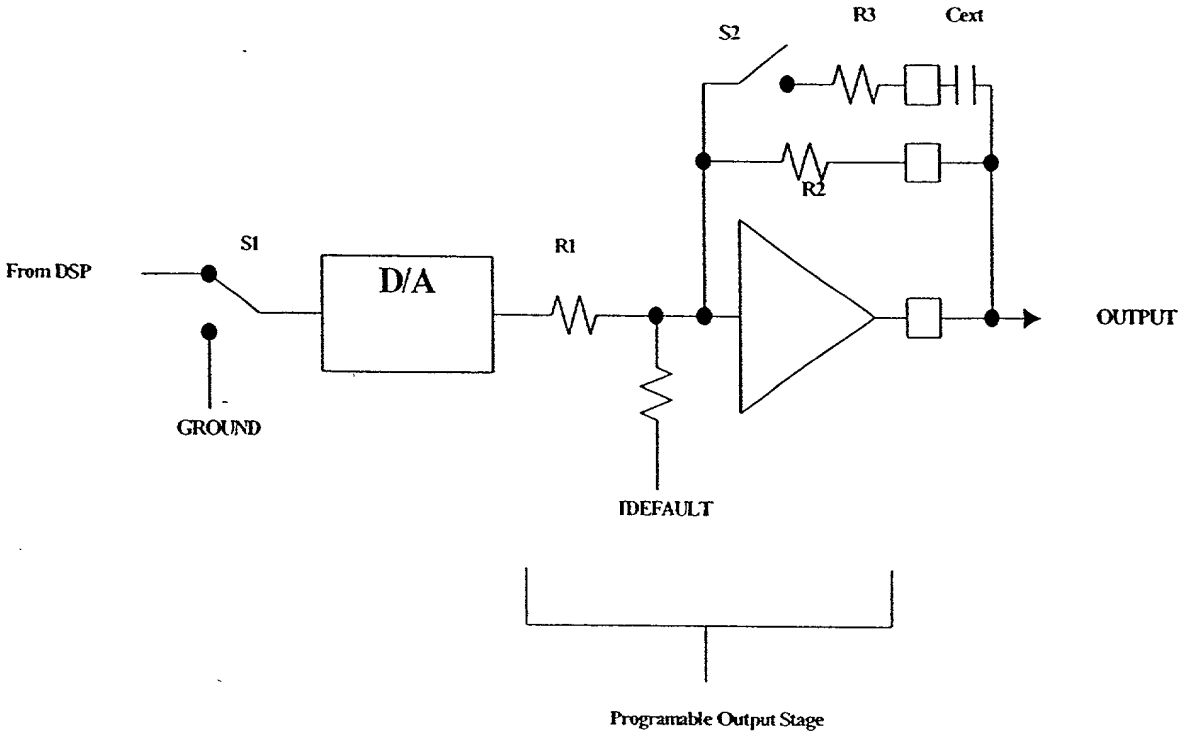
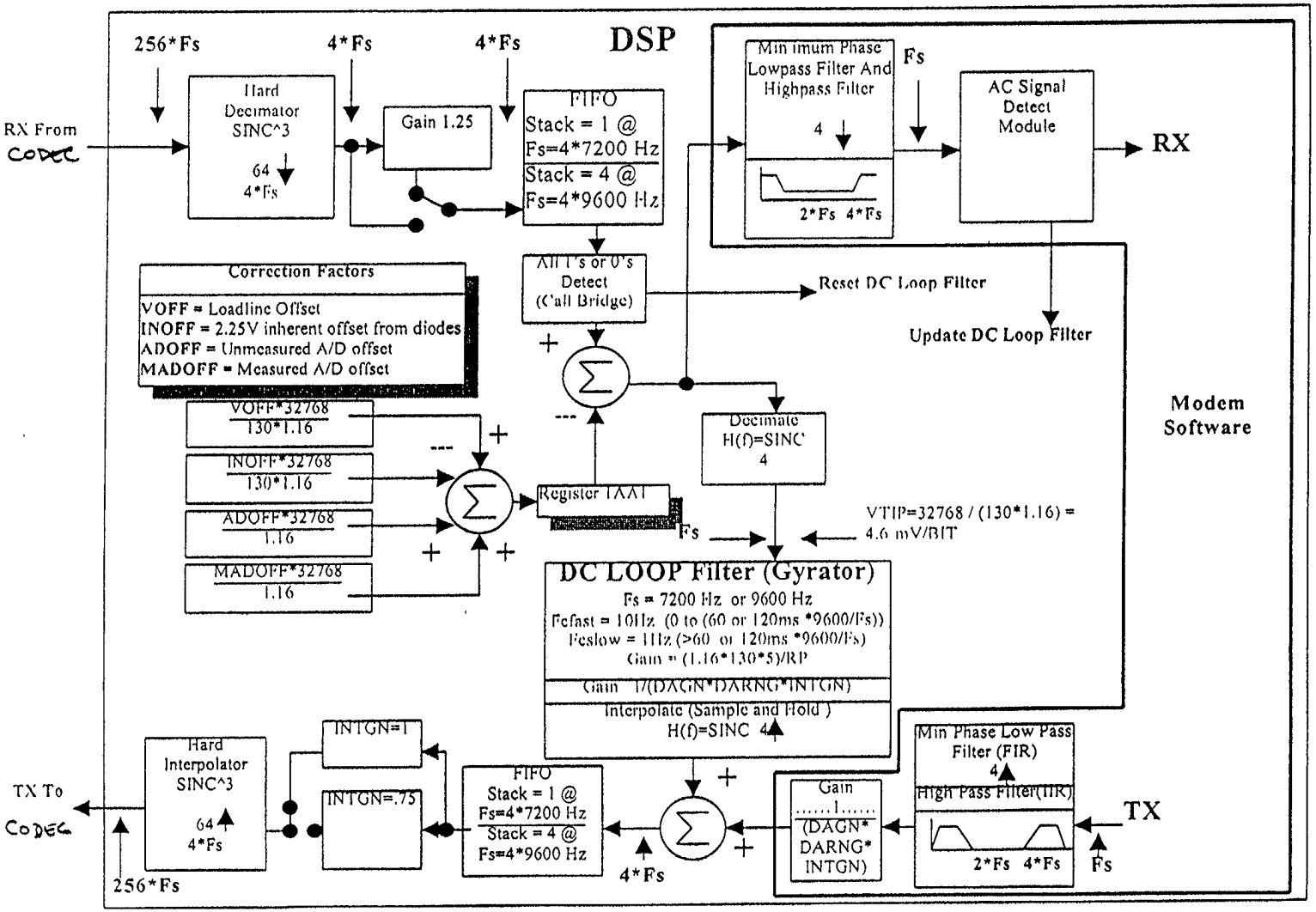


FIG. 4

Simplified D/A Path



DSP Based Gyrator Block Diagram

FIG. 5

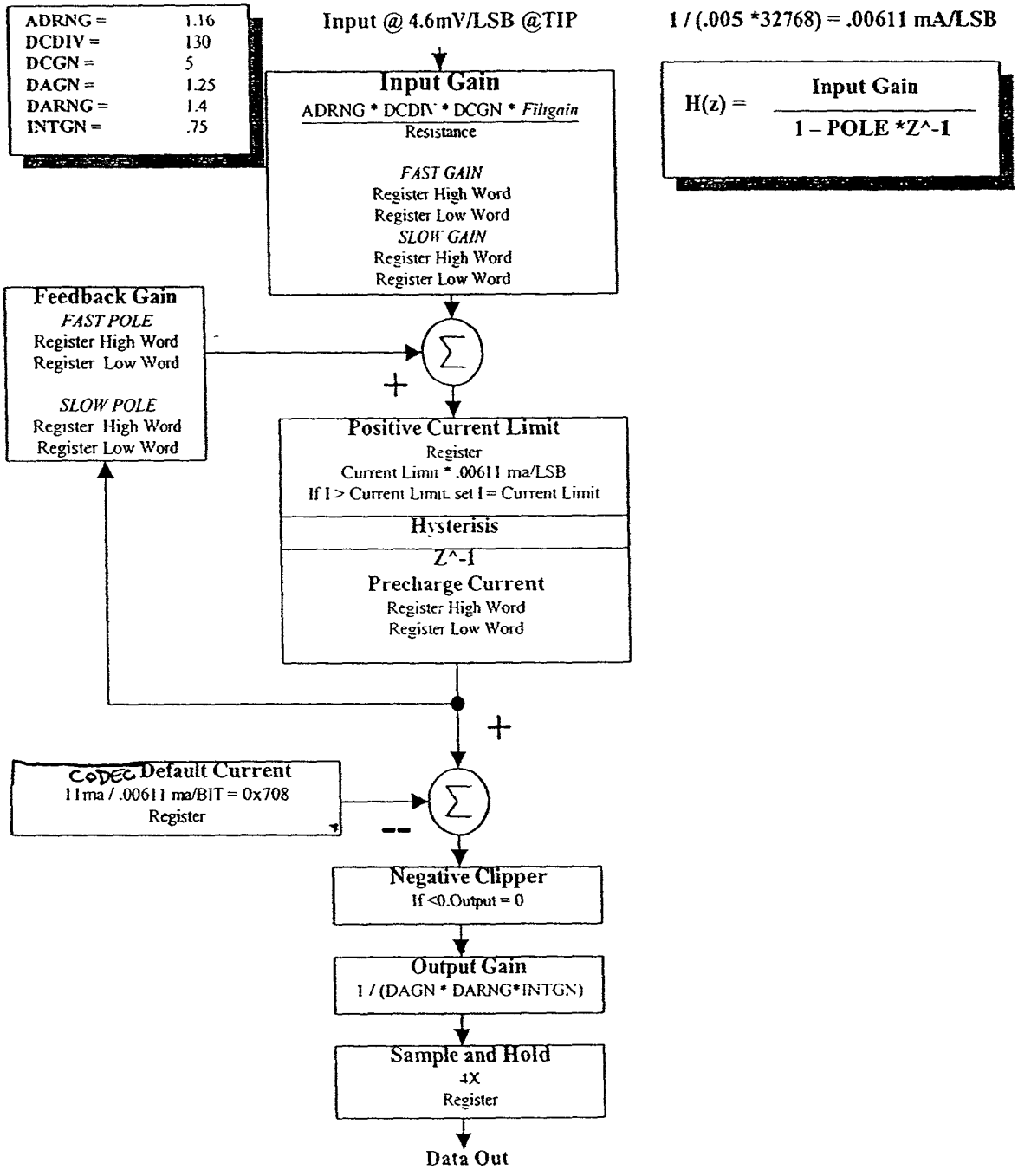

ADRNG = 1.16
DCDIV = 130
DCGN = 5
DAGN = 1.25
DARNG = 1.4
INTGN = .75
Input @ 4.6mV/LSB @TIP
1 / (.005 *32768) = .00611 mA/LSB
Input Gain
ADRNG * DCDIV * DCGN * Filtgain
Resistance
FAST GAIN
Register High Word
Register Low Word
SLOW GAIN
Register High Word
Register Low Word
H(z) = Input Gain / 1 – POLE *Z^-1
Feedback Gain
FAST POLE
Register High Word
Register Low Word
SLOW POLE
Register High Word
Register Low Word
Positive Current Limit
Register
Current Limit * .00611 ma/LSB
If I > Current Limit set I = Current Limit
Hysterisis
Z^-1
Precharge Current
Register High Word
Register Low Word
CODEC Default Current
11ma / .00611 ma/BIT = 0x708
Register
Negative Clipper
If <0.Output = 0
Output Gain
1 / (DAGN * DARNG*INTGN)
Sample and Hold
4X
Register
Data Out

FIG. 6

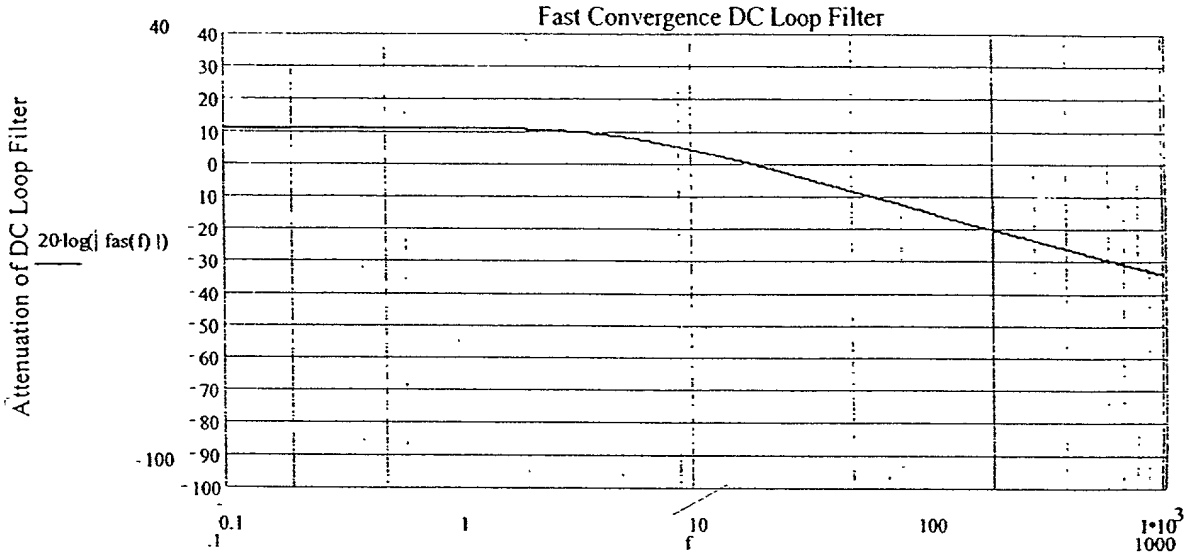


FIG. 7A

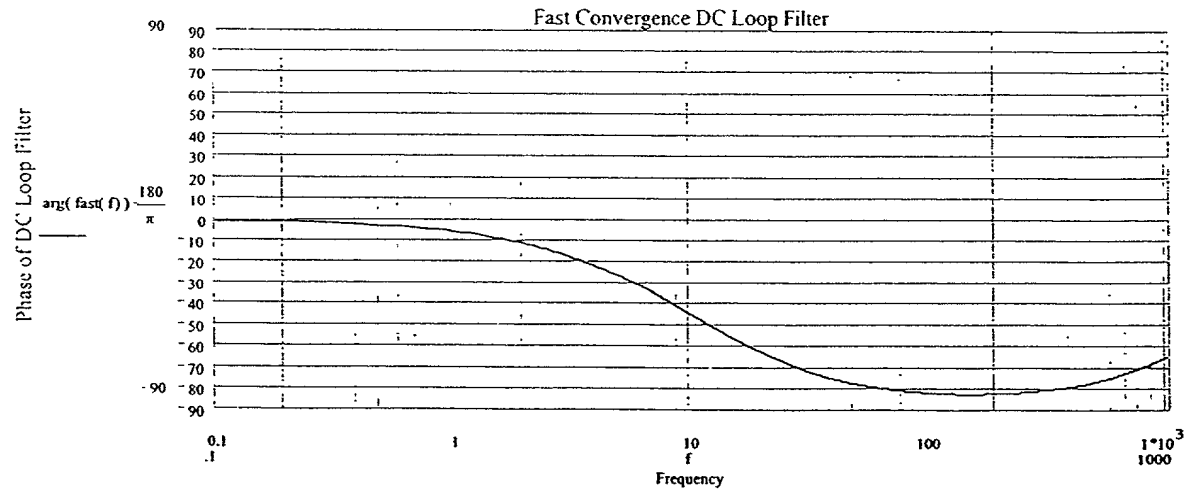


FIG. 7B

10 Hz Fast DC Loop Filter Gain and Phase

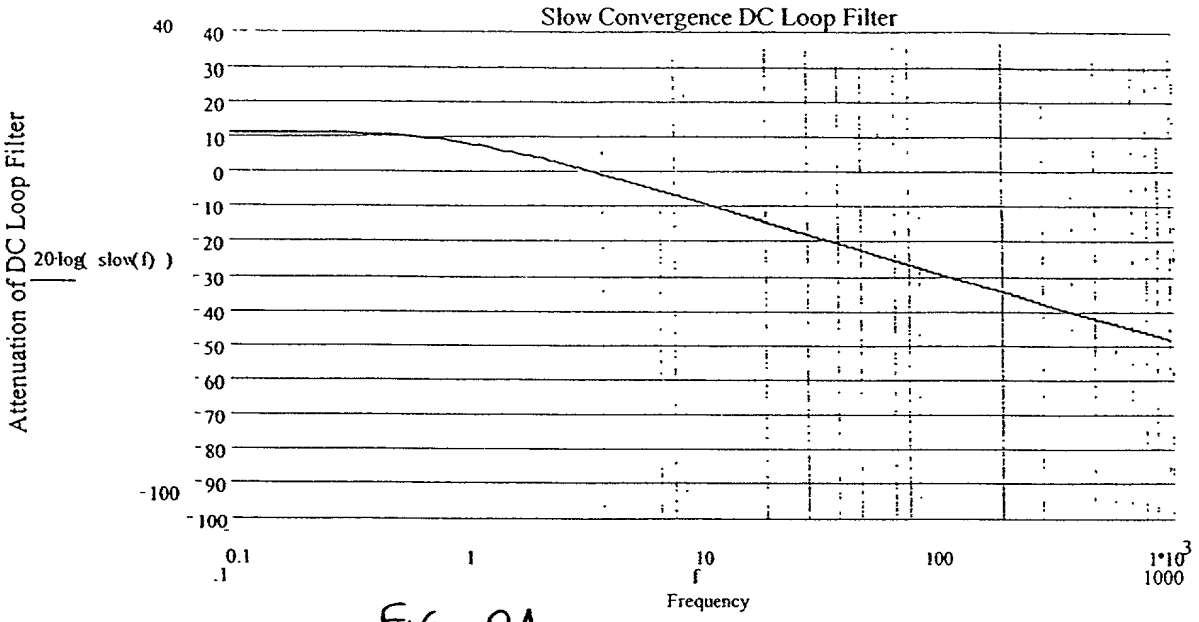


FIG. 8A

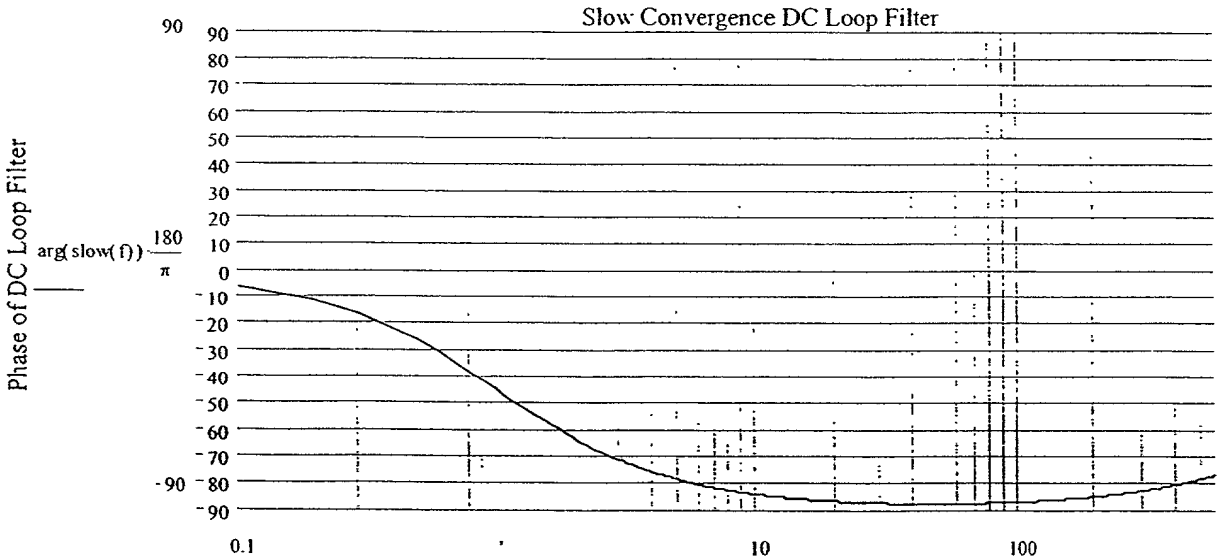
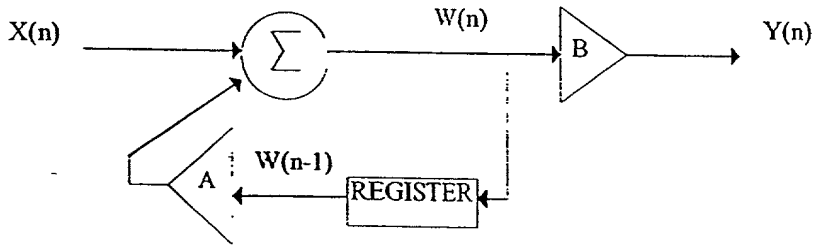


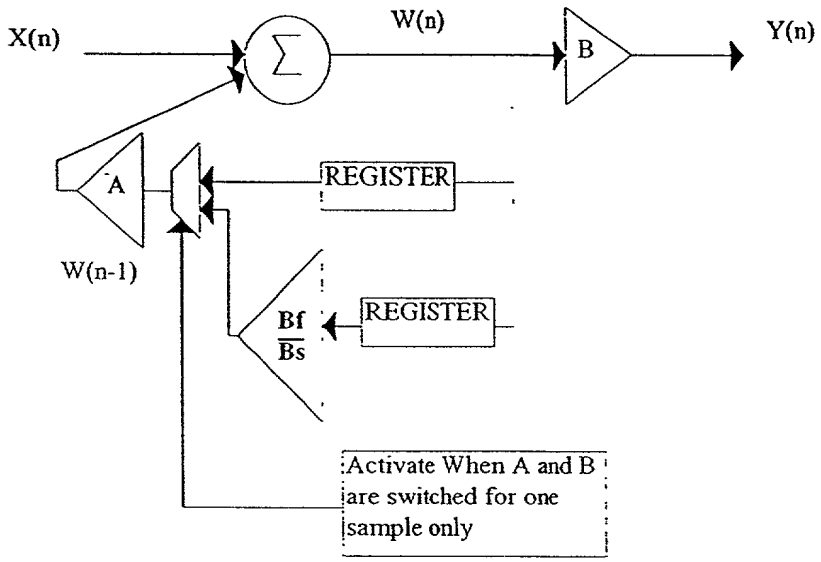
FIG. 8B

1 Hz Slow DC Loop Filter Gain and Phase



First Order Filter Topology

Fig. 9



Final Low Pass Topology with glitch removed

FIG. 10

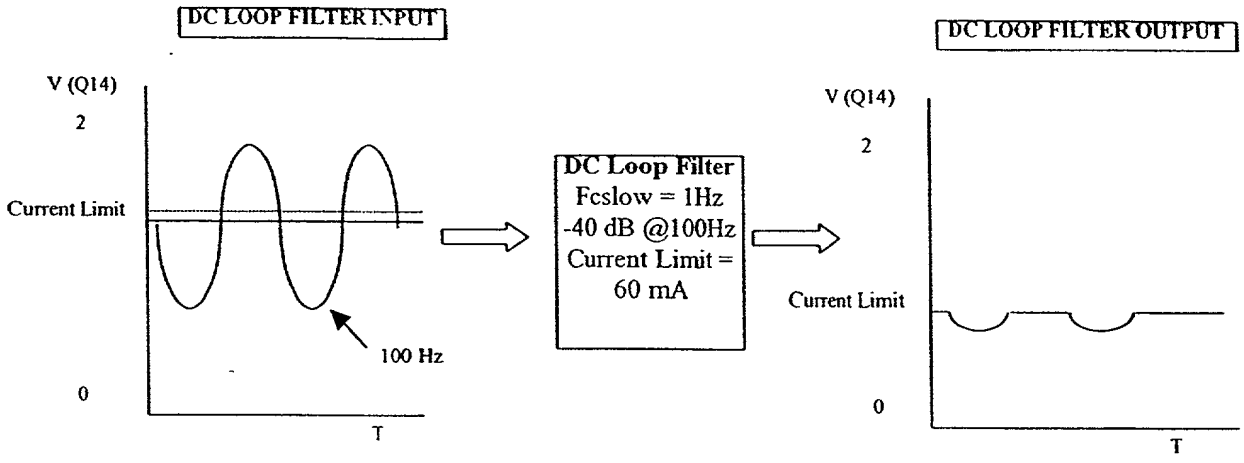


FIG. 11A

DC Loop Filter Without Hysterysis

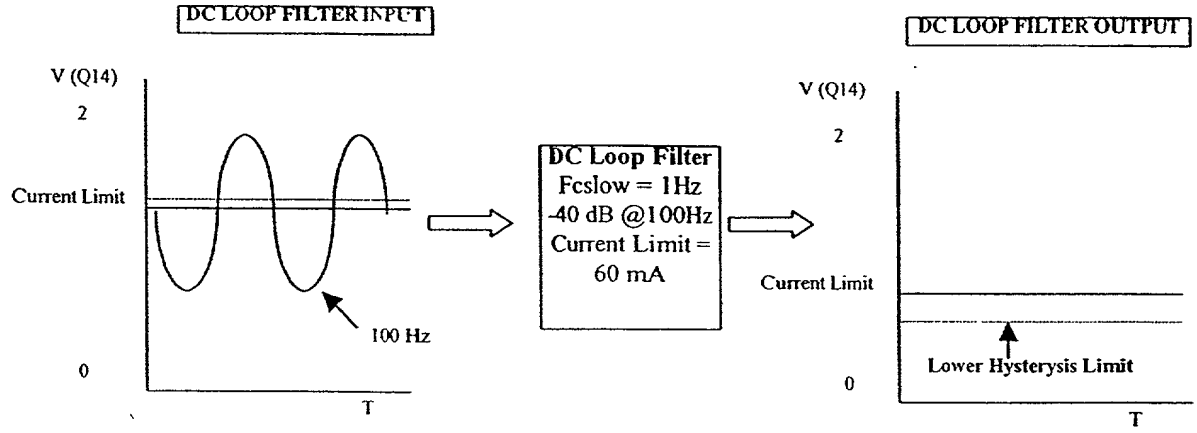


FIG. 11B

DC Loop Filter With Hysteresis

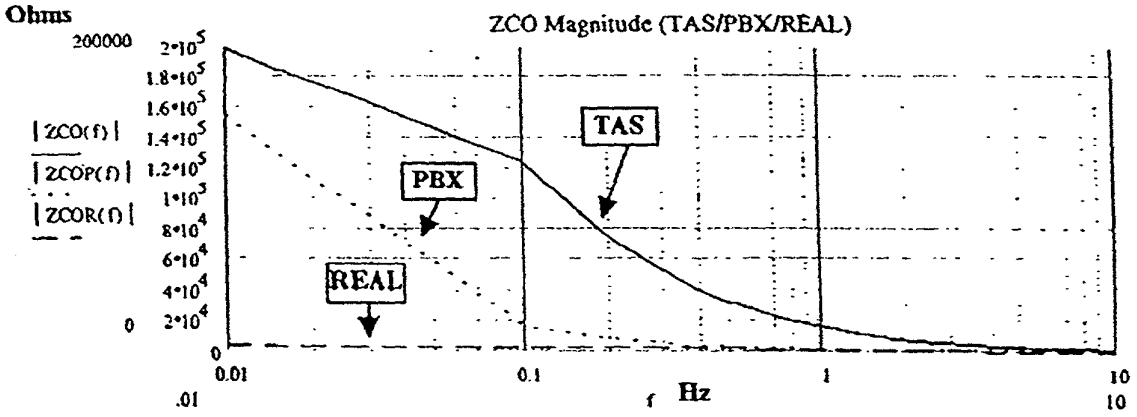


FIG. 12A

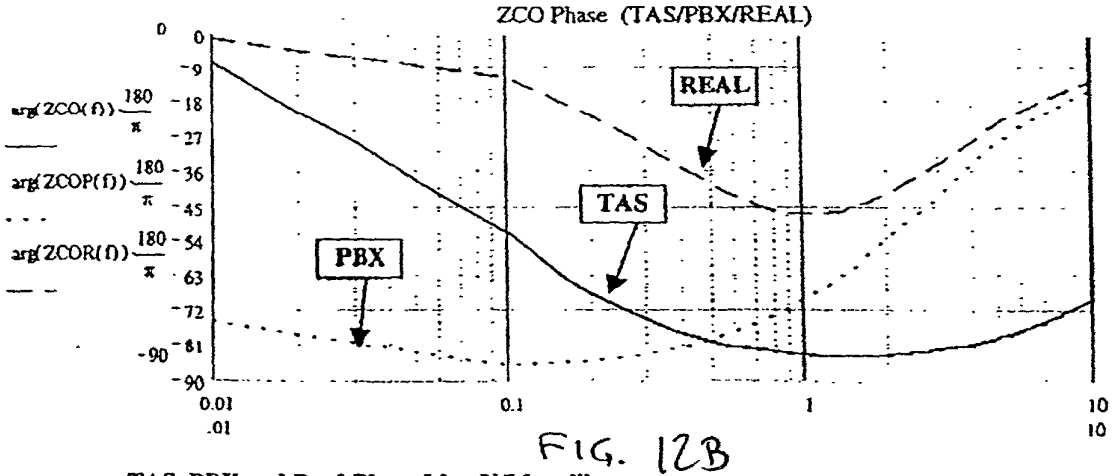


FIG. 12B

TAS, PBX and Real Phone Line V/I Loadlines

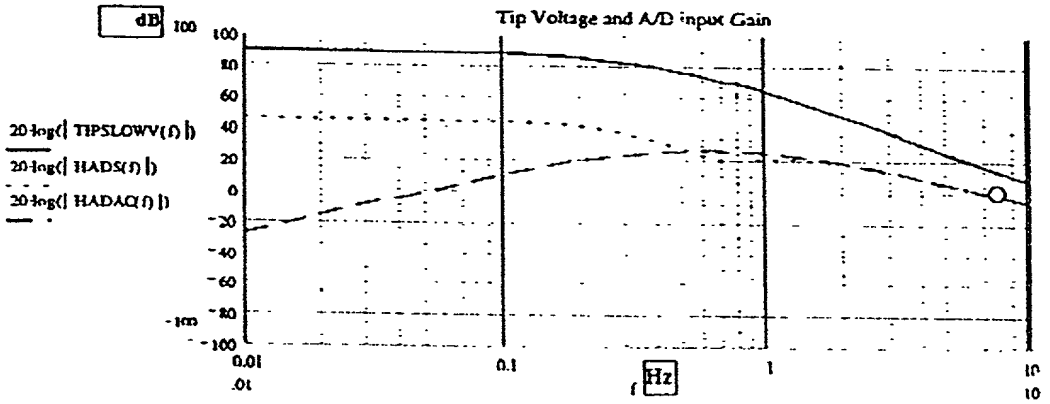


FIG. 13A

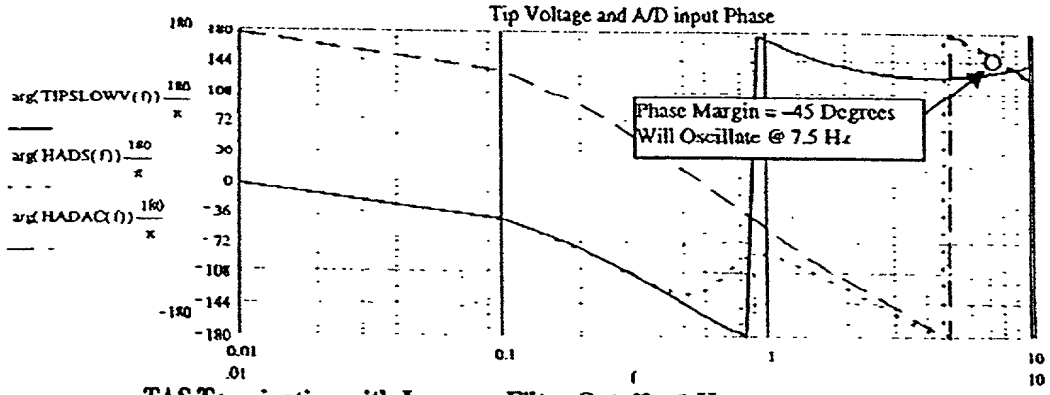


FIG. 13B

TAS Termination with Lowpass Filter Cutoff = 1 Hz

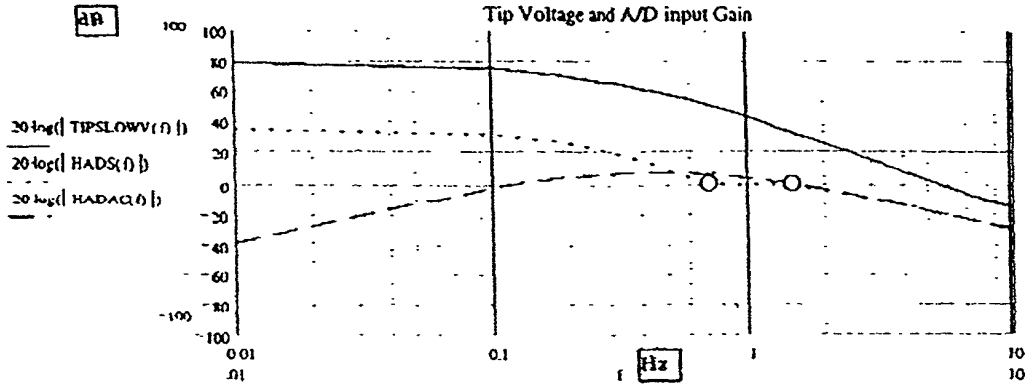


FIG. 14A

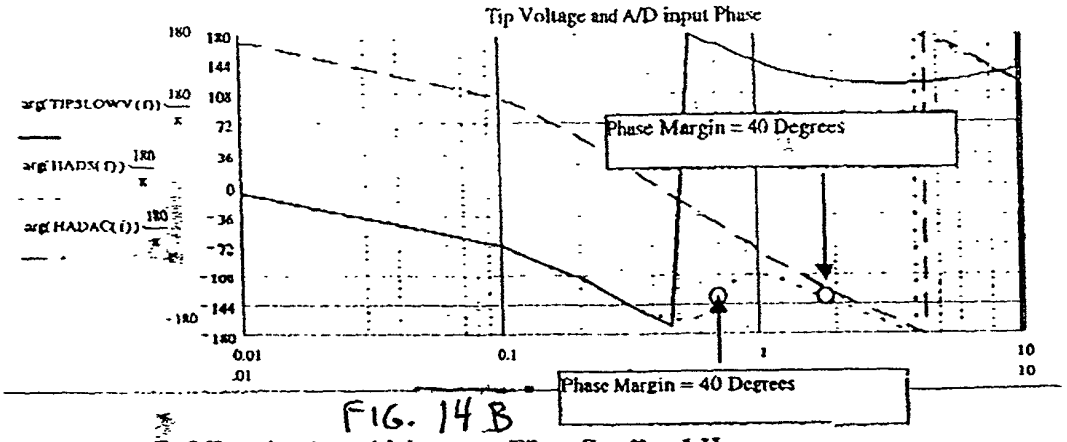


FIG. 14B

TAS Termination with Lowpass Filter Cutoff = .1 Hz

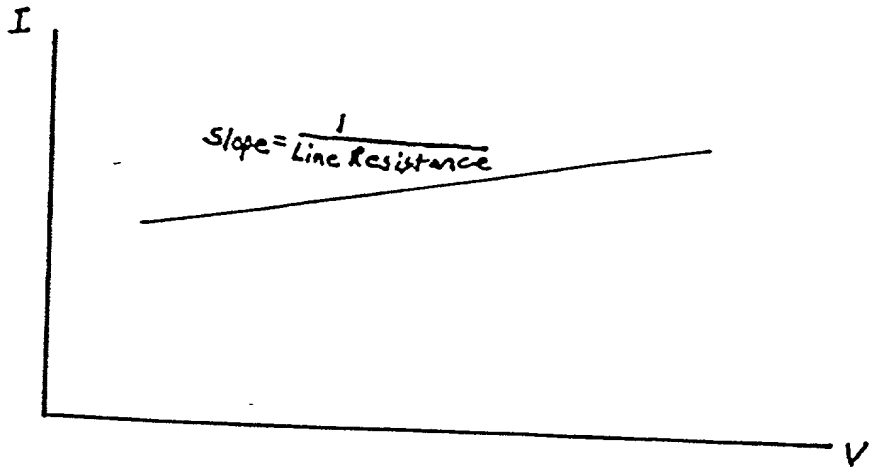


FIG. 15
(PRIOR ART)

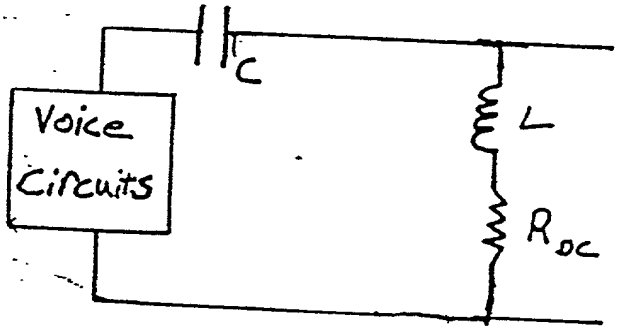


FIG. 16
(PRIOR ART)

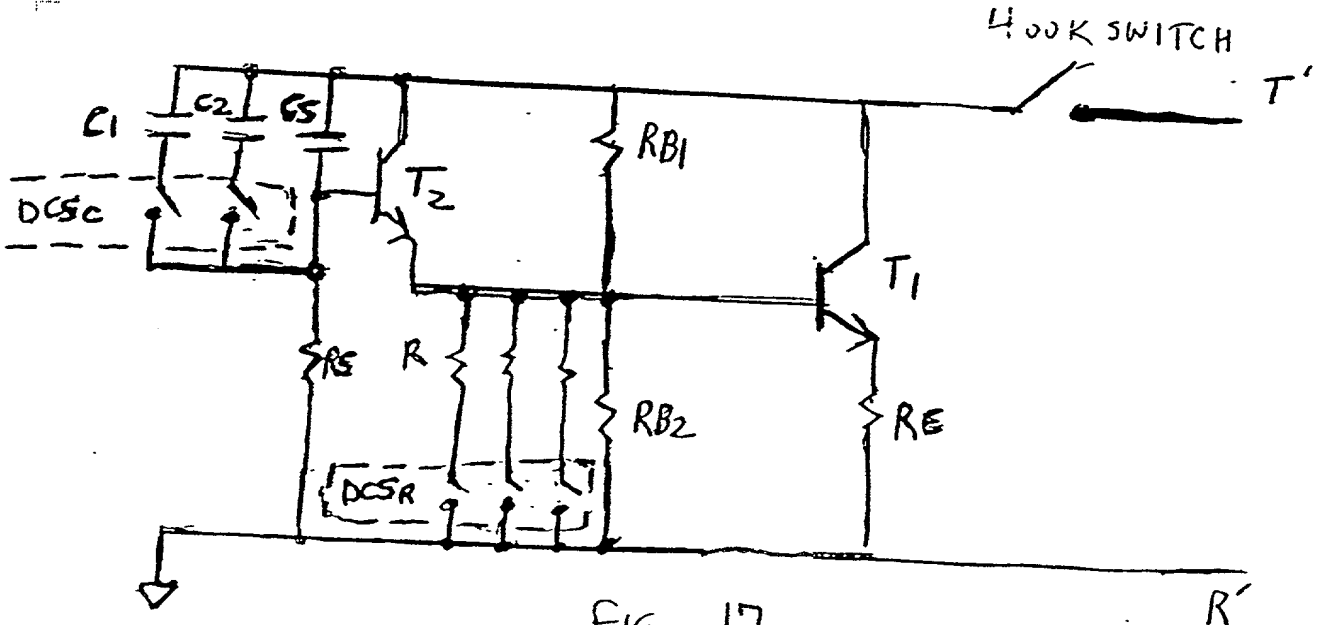
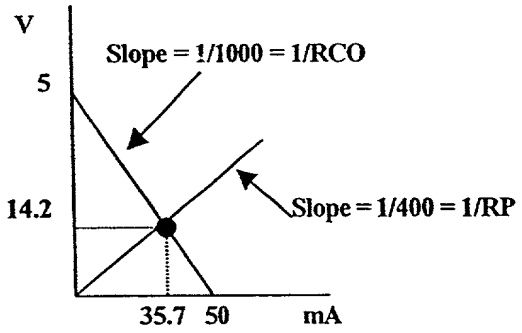


FIG. 17
(PRIOR ART)

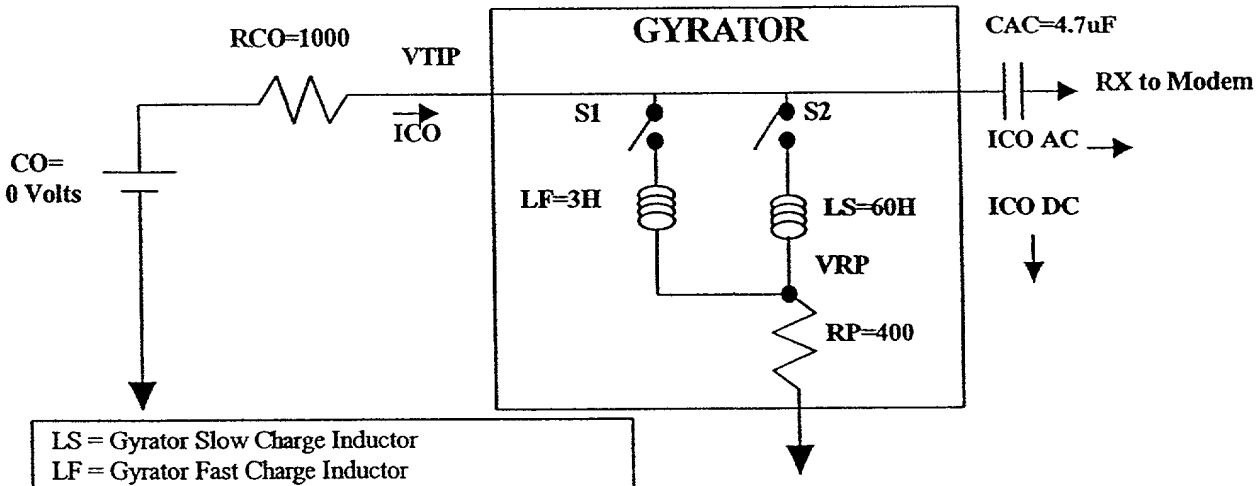
V/I Loadline



50 – ICO*RCO = ICO*RP =VTIP
ICO=14.27 mA
VP=35.7 Volts
Note: All results are at steady state

PRIOR ART

FIG. 18A



LS = Gyrator Slow Charge Inductor
LF = Gyrator Fast Charge Inductor
RP = Gyrator Impedance
CAC = AC coupling capacitor for AC modem signals
RCO = Central Office Resistance

Basic External Gyrator Example

FIG. 18B
PRIOR ART